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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,652	11/12/2003	Kang-Deog Suh	4591-344	8964

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EXAMINER	
NGUYEN, TAN	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/712,652	SUH ET AL.	
	Examiner	Art Unit	
	Tan T. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 11-16* is/are rejected.

7)☒ Claim(s) *6-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

2. The drawings are objected to because Fig. 1 should be labeled as --PRIOR ART--. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. Claims 5-10 are objected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 5, lines 6-7, it is not clear as to what Applicants mean by "generating program verification voltages selectively in response to the program verification

voltages. Should the program verification voltages [VRDV] are generated selectively in response to the program verification control signals [PGM_VFEN1] and [PGM_VFEN2] ?.

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-4 and 11-16 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-4 of U.S. Patent No. 6,853,585 (hereinafter U.S. Pat. No.'585). Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-4 of U.S. Pat. No. '585 recites the same elements in claims 1-4 and 11-16 of the present Application.

Regarding claim 1, of the present application, claim 1 of U.S. Pat. No, '585 recited a flash memory device comprising a memory cell array block including a plurality of memory flash memory cell, a program verify voltage generating unit (program verification voltage generator in the present application) capable of variably generating a program verify voltage (program verification voltages) that verifies flash memory cells

programming, a word line level selecting unit (word line level selector) capable of transferring the program verify voltage to the flash memory cells.

Regarding claim 2 of the present application, claim 2 of U.S. Pat. No. '585 recited the program verify voltage generating unit includes a PMOS transistor coupled at a first end to a power supply voltage, first to third resistors serially coupled between a second end of the PMOS transistor and a ground voltage. These first to third resistors correspond to the series of resistors in claim 2 of the present application. First and second NMOS transistors coupled across the first and second resistors, and responsive to a first and second program verify control signals, respectively. A comparator capable of comparing a voltage at a node between the first and second resistors with a reference voltage, the comparator having an output connected a gate of the PMOS transistor.

Regarding claim 3 of the present application, claim 3 of U.S. Pat. No. '585 recited the first and second program verify control signals are selectively activated to thereby fluctuate the program verify voltage.

Regarding claim 4 of the present application, claim 4 of U.S. Pat. No. '585 recited the word line level selecting unit applies a program voltage, a read voltage, and a pass or an erase voltage to a word line.

Regarding claim 11 of the present application, the first NMOS transistor in claim 2 of U.S. Pat. No. '585 is responsive to a first program verify control signal, the signal line for transferring the first program verify control signal corresponds to the claimed input. For the voltage generator in claim 11 and 14 of the present application, claim 2 of

U.S. Pat. No. '585 recited the program verify voltage generating unit includes a PMOS transistor which corresponds to the claimed serial transistor, first to third resistors serially coupled to the PMOS transistor, these resistors correspond to the claimed first and second resistors, first and second NMOS transistors correspond to the claimed first and second transistors. The word line level selecting unit in claim 1 of U.S. Pat. No. '585 corresponds to the claimed word line selector in claim 11 of the present application.

Regarding claim 12 of the present application, claim 2 of U.S. Pat. No. '585 recited a second NMOS transistor responsive to a second program verify voltage control signal, the signal line for transferring the second program verify control signal corresponds to the claimed second input

Regarding claim 13 of the present application, the first and second NMOS transistors in claim 2 of U.S. Pat. No. '585 correspond to the claimed transistors.

Regarding claim 15 of the present application, claim 2 of U.S. Pat. No. '585 recited a comparator capable of comparing a voltage at a node between the first and second resistors with a reference voltage.

Regarding claim 16 of the present application, claim 2 of U.S. Pat. No. '585 recited the output of the comparator connected a gate of the PMOS transistor which corresponds to the claimed serial transistor.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-5 and 11-16 are rejected under 35 U.S.C. 102(e) as being fully anticipated by Lee et al. (U.S. Patent No. 6,853,585).

Regarding claims 1 and 11, Lee et al. disclosed in Fig. 4 a flash memory device [400] comprises a memory cell array block [110], a program verify voltage generating unit [410] and a word line selecting unit [130] (column 4, lines 45-49), wherein the program verify voltage generating unit variably generates a program verify voltage that verifies flash memory cells programming (column 3, lines 18-20 and claim 1, lines 20-22). The signal line carries the first program verify control signal [PGM-VFEN1] (column 4, lines 61-62) corresponds to the claimed input.

Regarding claims 2 and 11-16, Lee et al. disclosed the program verify voltage generating unit [410] includes a PMOS transistor [413], first to third resistors [414, 415, 416] that are serially coupled between a power supply voltage [Vcc] and ground voltage [Vss], a first NMOS transistor [417] coupled to both ends of the first transistor [414] and a second NMOS transistor [418] coupled to both ends of the second resistor [415. The PMOS transistor [413] gates to an output of a comparator [412] for comparing a reference voltage [VREF] with an NA node voltage. The first NMOS transistor [417] gates to a first program verify control signal [PGM_VFEN1] to short the first resistor [414]. The second NMOS transistor [418] gates to a second program verify control signal [PGM_VFEN2] to short the second resistor [418] (column 4, lines 51-65).

Regarding claim 3, Lee et al. disclosed the program verify voltage generating unit [410] is selectively shorted depending on whether the first program verify control signal [PGM_VFEN1] or the second program verify control signal [PGM_VFEN2] is activated. Thus the level of a program a program verify voltage [VRDV] is high or low responsive to the control signals [PGM_VFEN1] and [PGM_VFEN2] (column 4, line 66 to column 5, line 4).

Regarding claim 4, Lee et al. showed in Fig. 4 the word line selecting unit [130] receives and transfers read voltage [VREAD], program voltage [VPGM], pass voltage {VPASS] or erase voltage to the word lines of the memory cell array block [110].

Regarding claim 5, as best understood, Lee et al. disclosed in Fig. 5 a program verify method comprising the steps of repeating a program unit loop cycle of applying predetermined programming voltages [VPGM1-VPGM9] to the flash memory cells, generating program verification voltages [VRDV1-VRDV3], verifying whether the flash memory cells are programmed or not in response to the program verification voltages, until the programming of the flash memory cells is completed, wherein the program verification voltages [VRDV1-VRDV3] are changed between two or more program unit loop cycles.

8. Claims 6-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Lee et al. (U.S. Pat. No. 585) failed to show the respective levels of the program verification voltages at (n-1)th, nth and (n+1)th program loop cycles.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arase, Devin et al., and Tanaka are cited to show memory devices having program verification circuit and method.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho, can be reached at (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tan T. Nguyen
Primary Examiner
Art Unit 2827
May 04, 2005